Appl. No. 10/761,702 Examiner: Warren, Matthew E, Art Unit 2815 In response to the Office Action dated March 10, 2005 Date: July 11, 2005 Attorney Docket No. 10113671

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (currently amended): A bit line contact structure, comprising:

a substrate having a transistor thereon, the transistor having a <u>raised</u> gate electrode, <u>a</u> drain region, and <u>a</u> source region;

a composite dielectric layer, sequentially having a first dielectric layer, barrier layer, and second dielectric layer, blanketly formed directly on the transistor, the first dielectric layer comprising a spin-coating material, the composite dielectric layer having an opening exposing the drain region; and

a conductive layer in the opening.

Claim 2 (canceled)

Claim 3 (original): The structure as claimed in claim 1, wherein the first dielectric layer is about 3000Å to 4000Å thick.

Claim 4 (original): The structure as claimed in claim 1, wherein the barrier layer is SiN.

Claim 5 (original): The structure as claimed in claim 1, wherein the barrier layer is about 100Å to 300Å thick.

Claim 6 (original): The structure as claimed in claim 1, wherein the second dielectric layer comprises an oxide layer.

Claim 7 (original): The structure as claimed in claim 1, wherein the second dielectric layer is about 1000Å to 3000Å thick.

Claim 8 (original): The structure as claimed in claim 1, wherein the conductive layer is doped polycrystalline silicon, tungsten, aluminum, or copper.

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Claim 9 (original): The structure as claimed in claim 1, wherein the first conductive layer is about 2000Å to 4000Å thick.

Claims 10-24 (canceled)

Claim 25 (new): A bit line contact structure, comprising:

a substrate having a transistor thereon, the transistor having a raised gate electrode, a drain region, and a source region;

a composite dielectric layer, sequentially having a first dielectric layer, barrier layer, and second dielectric layer, directly on the transistor, the first dielectric layer comprising polysilsequioxane, the composite dielectric layer having an opening exposing the drain region; and

a conductive layer in the opening.

Claim 26 (new): A bit line contact structure, comprising:

a substrate having a transistor thereon, the transistor having a raised gate electrode, a drain region, and a source region;

a composite dielectric layer, sequentially having a first dielectric layer, barrier layer, and second dielectric layer, directly on the transistor, the first dielectric layer comprising polyimide, the composite dielectric layer having an opening exposing the drain region; and

a conductive layer in the opening.

Claim 27 (new): The structure as claimed in claim 26, wherein the first dielectric layer comprises fluorinated polyimide.